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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,436	01/12/2004	Christopher Alan Greer	200312141-1	2182

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,436	GREER ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received January 12, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement(s) is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuskin (US Patent No. 6,829,683).

For claim 1, Kuskin discloses a method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system, comprising sending a request transaction for ownership of a cache line from a first processor to a memory unit (a method for transferring ownership of data in a distributed shared memory system that includes generating a return request at a processor to return a cache line, col. 1, lines 38-41),

determining from the memory unit which one of a plurality of processors other than the first processor has ownership of the requested cache line and sending a recall transaction to a second processor (a memory directory interface unit determines which processors in the system maintain a copy of the cache line, col. 26, lines 34-35), and

sending the requested cache line with ownership from the second processor to the first processor in response to the recall transaction (a processor may request data from any memory within the system through accesses to the memory directory interface unit corresponding to the memory containing the data, and if the data is held in the cache of another processor, the data may be retrieved from the other processor according to a protocol scheme, col. 2, lines 63-67 and col. 3, lines 1-2).

For claim 2, Kuskin discloses sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor (a return request is forwarded from a processor interface associated with a first processor to a memory directory, which generates an intervention request that is forwarded to the processor interface, which provides an intervention response to the intervention request to a second processor prior to processing of the return request, the response including the cache line, col. 1, lines 37-50; memory may respond to a request through a direct reply wherein a read data or write acknowledge reply is sent, col. 16, lines 51-55).

Claim 3 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 4 is rejected using the same rationale as for the rejection of claim 2 above.

For claim 5, Kuskin discloses ownership of a cache line from a first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line from a third processor (if there is a writeback or relinquish outstanding, no intervention response needs to be issued because the presence of the writeback or relinquish indicates that the processor no longer holds the cache line, col. 22, lines 1-4; if a processor drops a cache line, the rest of the system does not become aware of the dropping of the cache line and interventions for the cache line will continue until a relinquish message is sent to let the system know that a processor is giving up ownership of the cache line, col. 25, lines 24-30).

Claim 18 is rejected using the same rationale as for the rejections of claims 1 and 2 above. Further, it is to be noted that the processes described in this claim are inherently provided in the form of transaction lines.

Claim 19 is rejected using the same rationale as for the rejections of claims 3 and 18 above.

Claim 20 is rejected using the same rationale as for the rejections of claims 3, 4 and 18 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuskin (US Patent No. 6,829,683) in further view of Bauman et al (US Patent No. 6,981,106).

For claim 6, Kuskin discloses the invention as per rejection of claim 1 above. Kuskin, however, fails to disclose updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

Bauman, however, discloses when a cache line is stored within a cache, a new entry is created with a tag RAM by storing the block address of the cache line at the addressable location referenced by the set address (col. 4, lines 47-51).

Kuskin and Bauman are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include updating a tag to reflect transfer of ownership because this would aid in managing data stored within a main memory (abstract), as taught by Bauman.

For claim 7, Kuskin discloses the invention as per rejection of claim 1 above. Kuskin, however, fails to disclose a computer system uses a directory-based cache coherency scheme.

Bauman, however, discloses a directory-based coherency mechanism is utilized to manage memory data (col. 1, lines 20-22).

Kuskin and Bauman are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include a directory-based cache coherency scheme because this would aid in managing memory data (col. 1, lines 20-22), as taught by Bauman.

Claim 17 is rejected using the same rationale as for the rejections of claims 1-4 and 6 above.

Claim 21 is rejected using the same rationale as for the rejections of claims 7 and 18 above.

6. Claims 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuskin (US Patent No. 6,829,683) in further view of McCracken (US Patent No. 6,381,681).

For claim 8, Kuskin discloses the invention as per rejection of claims 1 and 2 above. Kuskin, however, fails to disclose these steps for processors and cache lines that are contained within cell divisions.

McCracken, however, discloses each cell of a shared memory multiprocessor system may include any suitable number of processors and clusters, each representative processor includes an associated cache and is coupled to a memory controller through which it acquires access to memory pages, each memory page has a set of cache lines available for acquisition by other processors so that other processors may share memory pages, and each memory page includes a memory data and a memory directory which tracks information related to a memory page such as the

current state of each cache line, what processors are associated with cache lines, and other memory information (col. 3, lines 20-32).

Kuskin and McCracken are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include cell divisions because this would allow for separate acquire and release protection and because memory updates from processors within a cell common to a shared memory page being updated may occur immediately and reduce processing overhead associated with memory coherency (col. 2, lines 29-40), as taught by McCracken.

For claim 9, the combined teachings of Kuskin and McCracken disclose the invention as per rejection of claims 1, 2 and 8 above. McCracken further discloses a method wherein m = n = p (the multiprocessor system may include any suitable number of processors and any suitable number of cells, col. 3, lines 15-16; each cell may include any suitable number of processors, col. 3, lines 20-21).

Claim 10 is rejected using the same rationale as for the rejections of claims 8 and 9 above.

Claim 11 is rejected using the same rationale as for the rejections of claims 8 and 9 above.

Claim 12 is rejected using the same rationale as for the rejections of claims 8 and 9 above.

Claim 13 is rejected using the same rationale as for the rejections of claims 2 and 8 above.

Claim 14 is rejected using the same rationale as for the rejections of claims 4 and 8 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 5 and 8 above.

Claim 16 is rejected using the same rationale as for the rejections of claims 6 and 8 above.

Citation of Pertinent Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McAllister et al (US PGPub No. 20030056068) discloses a memory controller generating a transaction requesting one of the data lines to one of a plurality of modules when the module has a private or shared copy of the data line, and returning the data line or a response indicating that no copy of the line exists, and a code identifying the module requesting the data line.

Baumgartner et al (US Patent No. 6,275,907) discloses cache hierarchies that hold copies of requested cache lines as indicated by coherency responses received in request transactions in a non-uniform memory access computer system with a plurality of processing nodes and a node interconnect.

Gaither et al (US Patent No. 6,868,481) discloses a computer system maintains a list of a global ownership tag list for all cache lines in the eystem for which a cache has ownership, and that lines may be requested and shareable by devices.

Okochi et al (US PGPub No. 20040024839) discloses a multiprocessor system in which transactions may request a data transfer or invalidate cache data, and sending of data in response to a data transfer request.

Contact Information

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

3-24-06

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PRIMARY EXAMINER